Numerical Modeling of Underfill Resin Cure Evolution during Chip-Scale-Packaging

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SUMMARY: In flip-chip packages the chip is mounted directly on to a substrate using a grid-array of solder bumps. In order to minimize the thermal stress, it is necessary to use glass-filled epoxy encapsulant, traditionally known as 'Underfill', to improve the reliability of flip-chip solder joint interconnections. By applying an underfill encapsulant into the gap between the IC chip and the substrate, the thermal stress on the solder joints during each temperature excursion can be uniformly dispersed throughout the encapsulated structure, leading to an enhanced improvement o the fatigue durability. In an actual manufacturing process establishing efficient curing of the underfill resin in the solder-reflow oven is of paramount importance, as it is directly linked to the fatigue reliability of the part. Unfortunately, there are a number of parameters, such as, curing kinetics of underfill resin, temperature profile in the reflow oven, solder bump temperature, and solder bump patterns that interact with each other in determining the degree of cue. The current work addresses the aspect of predicting the underfill resin cure during an actual manufacturing process, taking into account all the process variables that influence the underfill resin cure.

KEYWORDS: Underfill Resin Cure, Chip-Scale-Packaging, Degree of Cure, Curing Kinetics, Solder Temperature, Reflow Oven Temperature Profile

INTRODUCTION

Over the last few decades, the microelectronics industry, in the form of computer and communication devices for the fast treatment of huge amounts of data has grown rapidly in size. Thus, integrated circuits (ICs) with high performance are in demand [1 - 3].

Flip chip assembly technology was originally developed in the early 1960s with IBM's Controlled Collapse Chip Connection process also known as C4. An integrated circuit chip is placed with its active face down onto a ceramic substrate, and electrical/mechanical connections are made with both the topside metallurgy (TSM), and ball limiting metallurgy (BLM). In recent years, flip chip assembly has evolved quite rapidly.

In contrast to the classic C4 process, state-of-the-art flip-chip assembly uses organic substrates in what is known as Flip Chip on Board (FCOB) or Direct Chip Attach (DCA) technology. In general, the assembly processes for these technologies are both costly and time consuming.

The direct attachment of a solder-bumped flip chip to an organic substrate requires the use of an underfill encapsulant to enhance the reliability of the flip-chip assembly.

An underfill with a high modulus, a coefficient of thermal expansion (CTE) matching that of the organic substrate, and with good adhesion to both the substrate (with and without solder mask) and the outermost passivation layer of the silicon die are required [4, 5]. By applying an underfill encapsulant into the gap between the IC chip and the substrate, the stress on the solder joints during each temperature excursion can be uniformly dispersed throughout the encapsulated module, leading to an enhanced improvement in the reliability.

Unfortunately, flip chip on board processing has yet to become a low cost, high throughput process compatible with high volume surface mount processing. Due to the advent of numerous classes of underfill material, varying in flow, curing characteristics, and also different manufacturing processes, it is essential to develop a design tool to facilitate prediction of cure behavior during an actual manufacturing process.

The current work addresses the aspect of underfill resin cure during an actual manufacturing process, taking into account all the process variable, such as underfill cure kinetics, solder bump temperature, temperature in reflow oven, and solder bump configurations, that influence the resin cure. The numerical tool developed gives an easy to use tool for process engineers to control and fine-tune the multiple, interacting process variables for efficient manufacturing of reliable packages.

RESULTS AND DISCUSSIONS

The manufacture of Chip-Scale packages takes place in 4 distinct steps:

1. Alignment and placement of the IC chip to the substrate;
2. Solder reflow cycling and flux residue cleaning
3. Dispensing underfill encapsulant on one or two edges of the assembly followed by capillary flow to fill the gap between the chip and the substrate;
4. Cure reaction of the underfill encapsulant in a solder reflow oven.

Theoretical Background

For the purpose of analyzing the cure process during manufacture, we consider the case of a completely filled underfill condition, which is passed through a reflow oven with a programmed heating profile. Fig. 1 shows the pictorial representation of the physics of the problem.

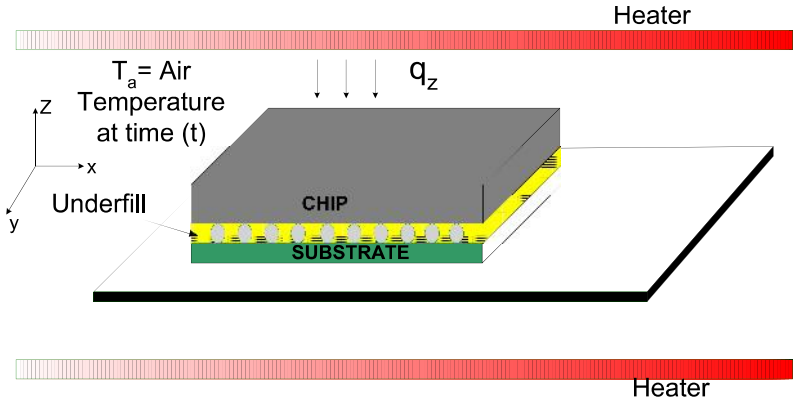

Fig. 1 Pictorial representation of the physics of the problem in reflow-oven

The temperature distribution, the degree of cure of the resin inside the flip-chip depends on the rate at which heat is transmitted from the environment into the material. The temperature inside the resin can be calculated using the law of conservation of energy together with an appropriate expression for the cure kinetics. The individual governing equations within the substrate, chip, and underfill resin are given below:

(a) Internal governing equations

$$\rho C_p \left[\frac{\partial T(x,y,z)}{\partial t} \right] = k \nabla^2 T(x,y,z) \tag{1}$$

(b) In the resin

$$\rho C_p \left[\frac{\partial T(x,y,z)}{\partial t} \right] = k \nabla^2 T(x,y,z) + \dot{H}_r \tag{2}$$

where H_r is the rate of heat of reaction, C_p is the specific heat, ρ is the density, and k is the thermal conductivity of the material.

The rate of heat of reaction is given by the expression

$$\dot{H}_r = \rho \Delta H_r \frac{\partial \alpha}{\partial t} \tag{3}$$

where α denotes the degree of cure, and the rate of cure is given by the expression:

$$\frac{d\alpha}{dt} = k \alpha^m (1-\alpha)^n \tag{4}$$

Furthermore, the boundary condition between chip top surface and air is evaluated by Eqn. 5, indicated below.

$$q_z'' = h(T_s - T_\infty) \tag{5}$$

where h is the convention heat transfer coefficient, T_s is the temperature on top of the chip, and T_∞ is the temperature of the air.

In the current paper, 'Dexter 4531' was utilized as the model underfill. From the kinetic experiments, the following kinetic constants were obtained, which were applied in Eqn. 3, which are indicated in Table 1. Furthermore the total heat of reaction was found to be 109 J/g at 170°C.

For the purpose of our simulation a 'Finite Difference' numerical scheme was employed. The whole chip was discretized into a small mesh pattern, and the nodal values for temperature, and degree of cure were evaluated over the time period of 4 minutes following the programmed heater profile in the reflow oven. Furthermore, the solder geometry was approximated from a cylindrical geometry to a square block based on equivalent volume.

Table 1. Kinetic Constants for Dexter 4531 Underfill

Temperature (°C)	k	m	n
130	0.0674	0.7	0.64
150	1.16	0.586	1.49
170	1.21	0.629	3.13

Case Study

This simulation results presented in this paper was done to predict the degree of cure during the actual CSP manufacturing process implemented in a manufacturing process. For this case study, the dimensions of the CSP used are: chip = 10 mm x 12 mm, pitch of solder bumps = 0.94 mm, bump diameter = 0.38 mm, gap height = 0.25 mm, thickness of chip = 0.38 mm and thickness of substrate = 0.6 mm. In this case, the Dexter 4531 underfill resin was utilized, for which the kinetic rate constants are indicated in Table 1. Furthermore, in this the solder bump temperature was kept at 25^{o}C, and the curing was done in the solder reflow oven according to the prescribed reflow oven heating temperature profile.

First, the value of the convection heat transfer coefficient was ascertained to be 1018 W/m^{2}K, which was obtained by matching the simulated chip surface temperature close to that obtained from experiments. Fig. 2 shows the graphical representation of the % degree of cure at the end of 4 minutes. We first note that for all time periods the curing behavior is symmetric. Our results also show that the degree of cure is found to be maximum at the edges, and minimum at the center. Fig. 3 shows the plot of % degree of cure at 3 locations, namely inner, middle, and outer nodal locations. From Fig. 3, we note that after a period of 4 minutes we have a 70% cure near the edges, which gradually reduces to less than 30% at the center of the chip. Furthermore, in the center we observe that the cure is less than 10% for the first 3 minutes, and later during the last 1 minute the cure reaches to 23%. From this simulation, we clearly infer that in the current process implemented in this case study; underfill cure is either incomplete or insufficient.

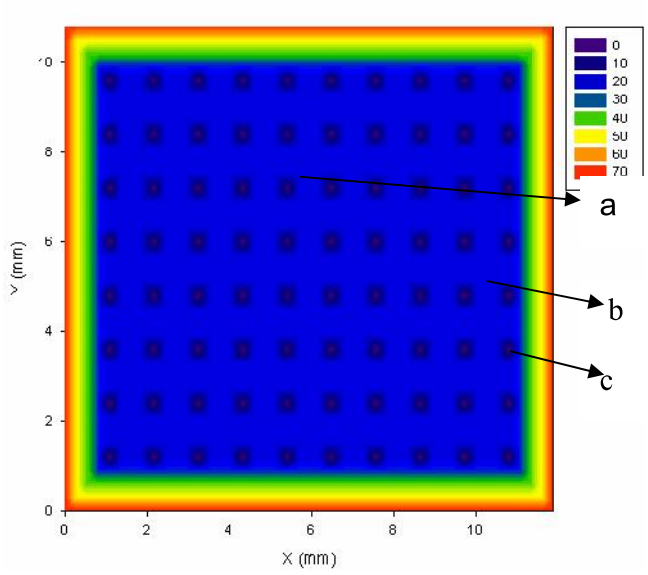

Fig. 2 Chip Surface Temperature Profile

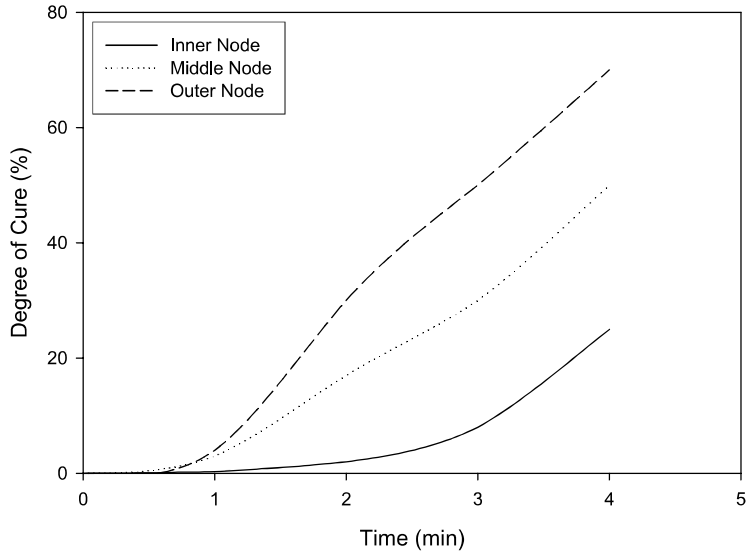

Fig. 10 % Degree of Cure at Outer, Middle and Inner Nodes for Case # 1

CONCLUSIONS

During the present study, an effort was undertaken to develop science-based numerical model to enhance the understanding of the underfill resin cure process that occur during microelectronics manufacturing. Models were developed to simulate the underfill curing process during CSP manufacturing process, which would facilitate efficient evaluation of a manufacturing process, and identify potential manufacturing processes relevant to chip-scale packaging process. This numerical scheme takes into account the heat conduction, and convection process in the actual manufacturing process, making the model more useful as an evaluation tool to assess part durability through process changes. Also, in this paper a case study was presented to illustrate the usefulness on this design tool.

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